Private Circuits
A Modular Approach

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Yuval Ishai

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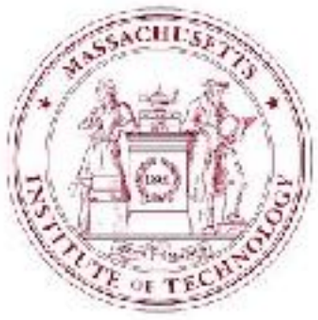

Surveillance Devices

Credit card details
SSN number
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Side Channel Attacks

Adversary can obtain partial information (leakage) about the computation

Leakage-Resilient Cryptography

GOAL

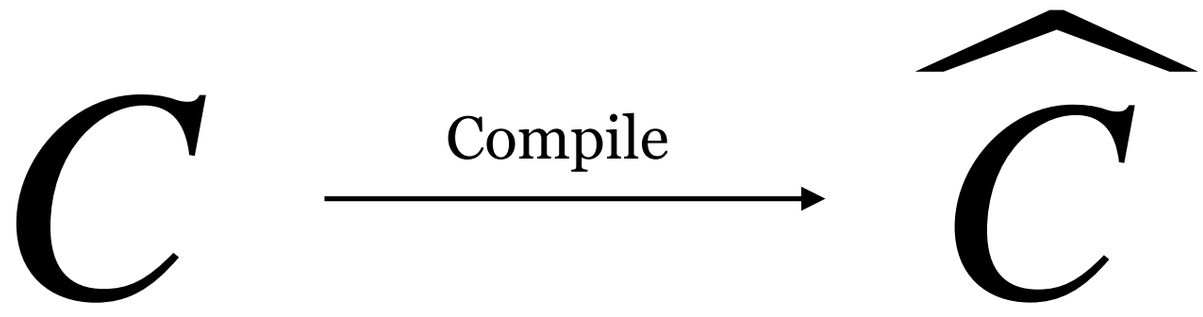
Protecting cryptographic schemes against

side-channel attacks

This Work:

Leakage-Resilient Circuit Compilers [ISW03]

Circuit Compilers



Circuit Compilers

$$C \xrightarrow{\text{Compile}} \widehat{C}$$

$$x \xrightarrow[\$\$]{\text{Encode}} \hat{x}$$

$$\widehat{C}\left(\hat{x}\right) \xrightarrow{\text{Decode}} C(x)$$

Remarks

- $C, \widehat{C}$ contain NAND gates

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- $\widehat{C}$ can contain random-bit gates

Leakage-Resilient Circuit Compilers

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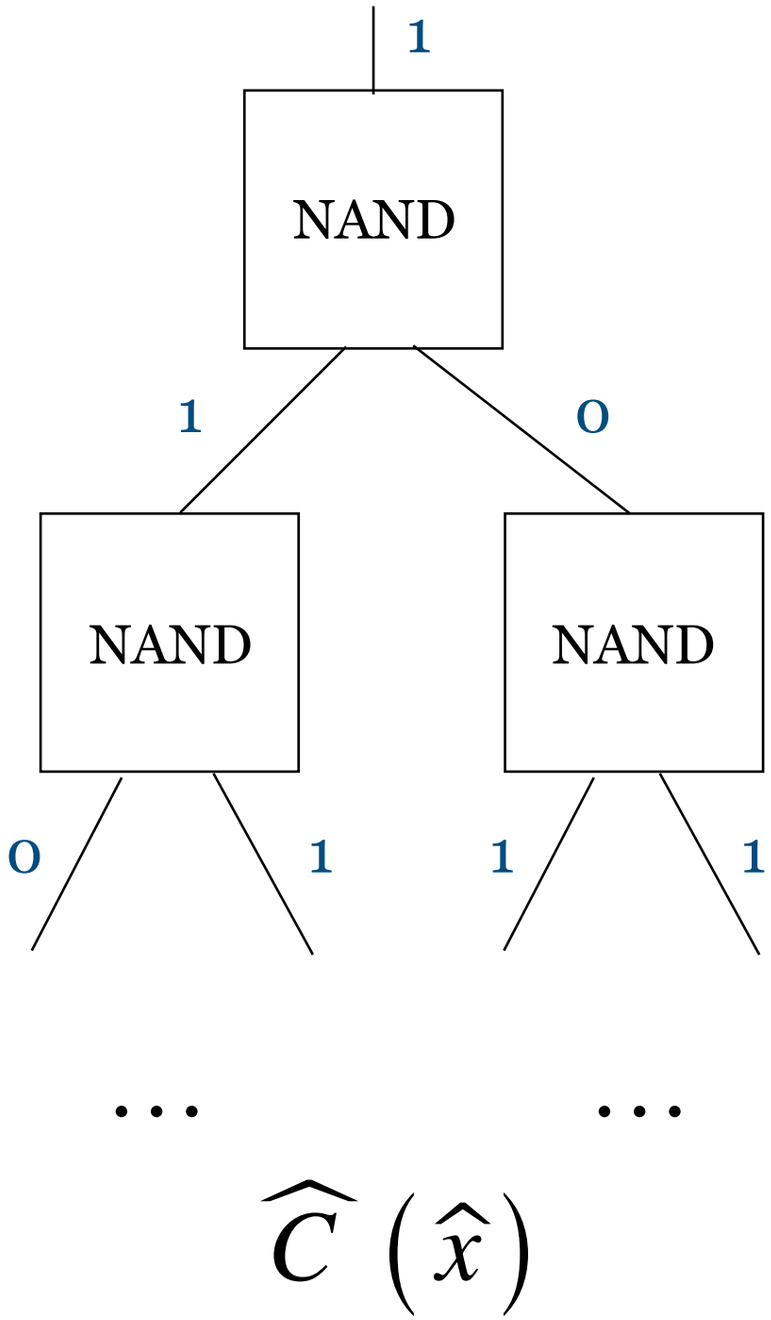
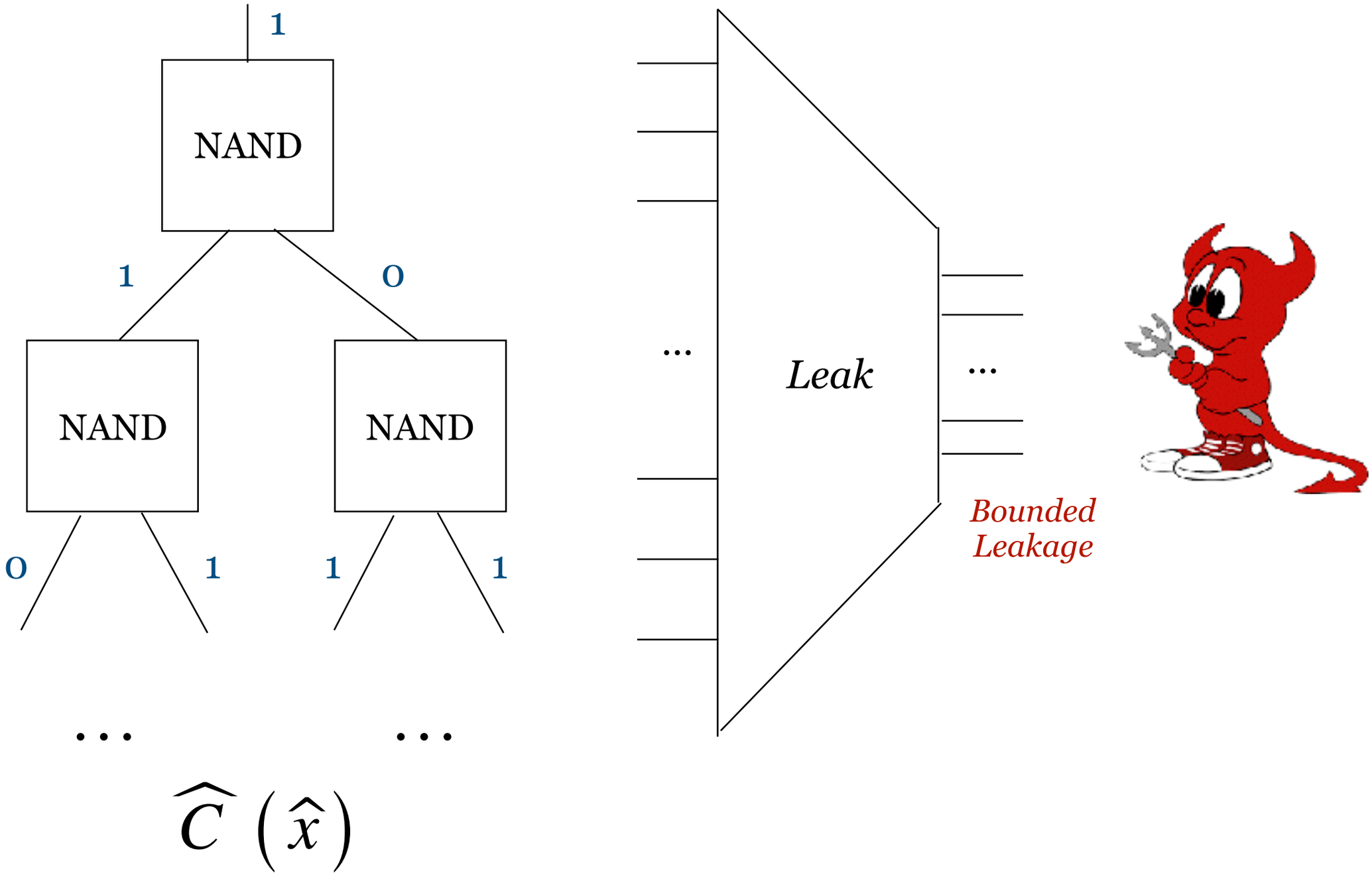


Leakage-Resilient Circuit Compilers



Leakage on computation of $\widehat{C}$ on $\hat{x}$

What is *Leak*?

- **Global leakage:** *Leak* is function of entire computation

- **Local leakage:** adversary has partial view of computation

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  - Wire-probing attacks [ISW03,…]

  - Split-state leakage-resilient compiler [MR03,DP08,GR12,…]

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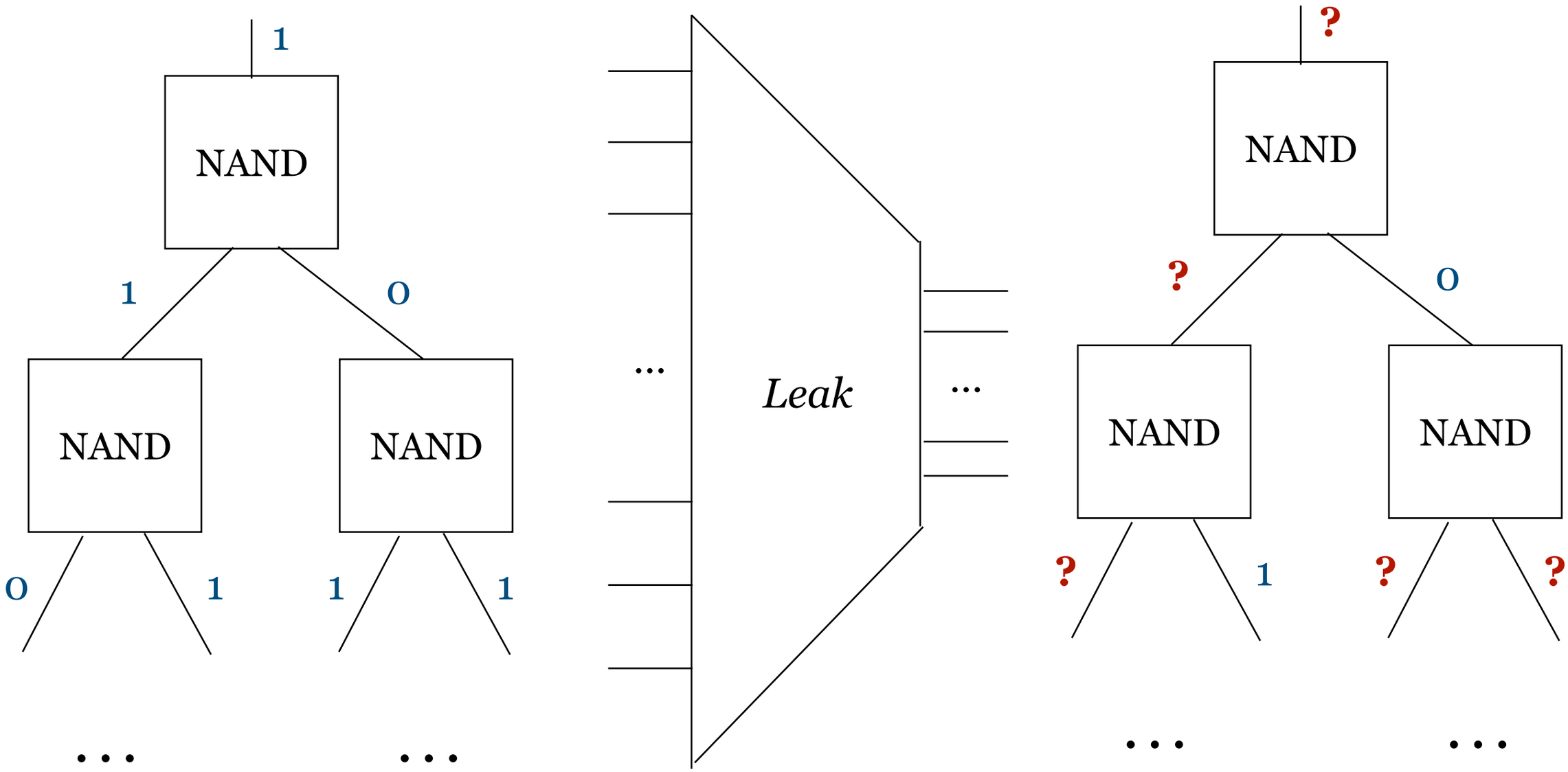
Wire-probing attacks [ISW03, …]



Subset of values in the computation leaked

Leakage-Resilience: Wire-probing attacks [ISW03,…]

Worst Case Leakage: threshold t

- Any t wires are leaked

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Following [ISW03], several works study this setting...
[RP10,KHL11,GM11,CPR13,CGPQR12,...]

MPC on Silicon

Applying MPC techniques to design secure hardware

Leakage-Resilience: Wire-probing attacks [ISW03,...]

Worst Case Leakage: threshold t

- Any t wires are leaked

Recent years: focus on randomness complexity

[IKLOPSZ13,BBPPTV16,BBPPTV17]

Randomness Complexity

Randomness Complexity = # of random-bit gates

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Results: Worst-Case Probing

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Leakage-Resilience: Random Wire-probing attacks

[ISW03,Ajtai10,ADF16]

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Probabilistic Leakage: parameterized by *(p,e)*

Real World	Ideal World
Every wire in $\widehat{C}\left(\hat{x}\right)$ leaked with probability p	Simulate leakage just given C

$$\approx_e$$

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Related to Noisy Leakage Model: [CJJR99,FRRTV10,DDF15,...]

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Random Wire-Probing Attacks

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- [ADF16]:

  - simplifies Ajtai's result

  - still uses heavy machinery (AG codes and expanders)

Results: Random-Wire Probing

Leakage-resilient circuit compiler against *(p,e)*-random probing attacks

- for some $0 < p < 1$

- e negligible in circuit size

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p = 0.000065

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Leakage-resilient circuit compiler against *(p,e)*-random probing attacks

- for some $0 < p < 1$

- e negligible in circuit size

- Simple composition-based approach; uses only elementary tools

Results: Random-Wire Probing

Leakage-resilient circuit compiler against *(p,e)*-random probing attacks

- for some $0 < p < 1$

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Large gates: construction with *p close to 1*

Leakage Tolerance

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$$\widehat{C}\left(\widehat{x}\right) = C(x)$$

Input encoding and Output decoding algorithms are identity functions

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This implies leakage-resilience!

Security Notions

A fraction of input and output will be leaked

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- Worst-case: *parameterized by t*

Leakage simulatable given

- *t* bits of input
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A fraction of input and output will be leaked

- Probabilistic: *parameterized by (p,**p'**,e)*

Leakage simulatable given
- every bit of input **x** w/ probability *p'*
- every bit of output **C(x)** w/ probability *p'*

Results: Leakage Tolerance

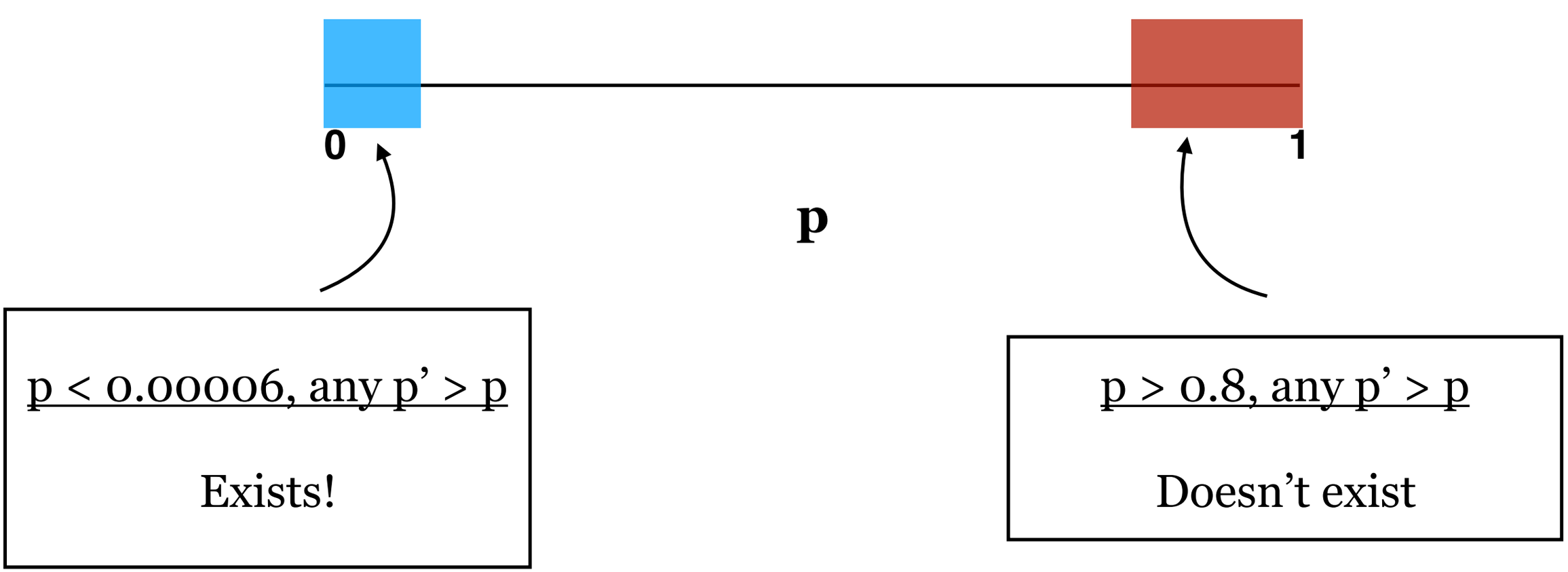
Worst Case: t-wire probing attacks

- *construction: randomness complexity* $t^{1+\varepsilon}$

- *lower bound: require at least* t *random-bit gates*

Results: Leakage Tolerance

Probabilistic Case: (**p**,**p'**,e)-random probing attacks



Techniques

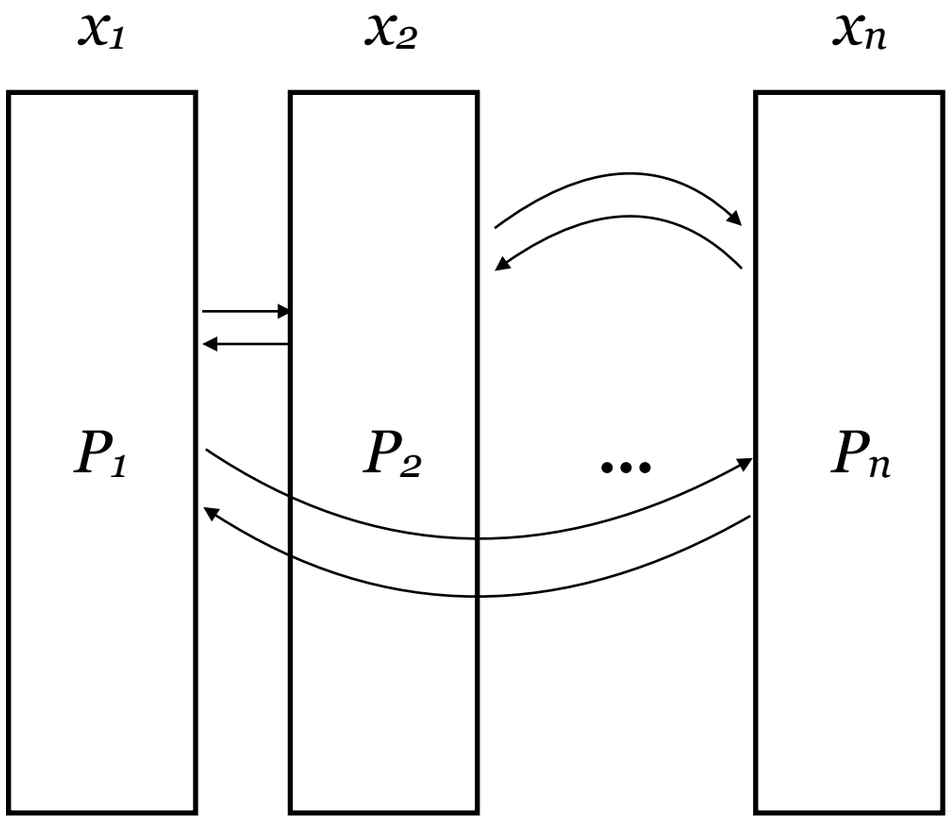
Goal for this talk

- Leakage-resilient circuit compiler

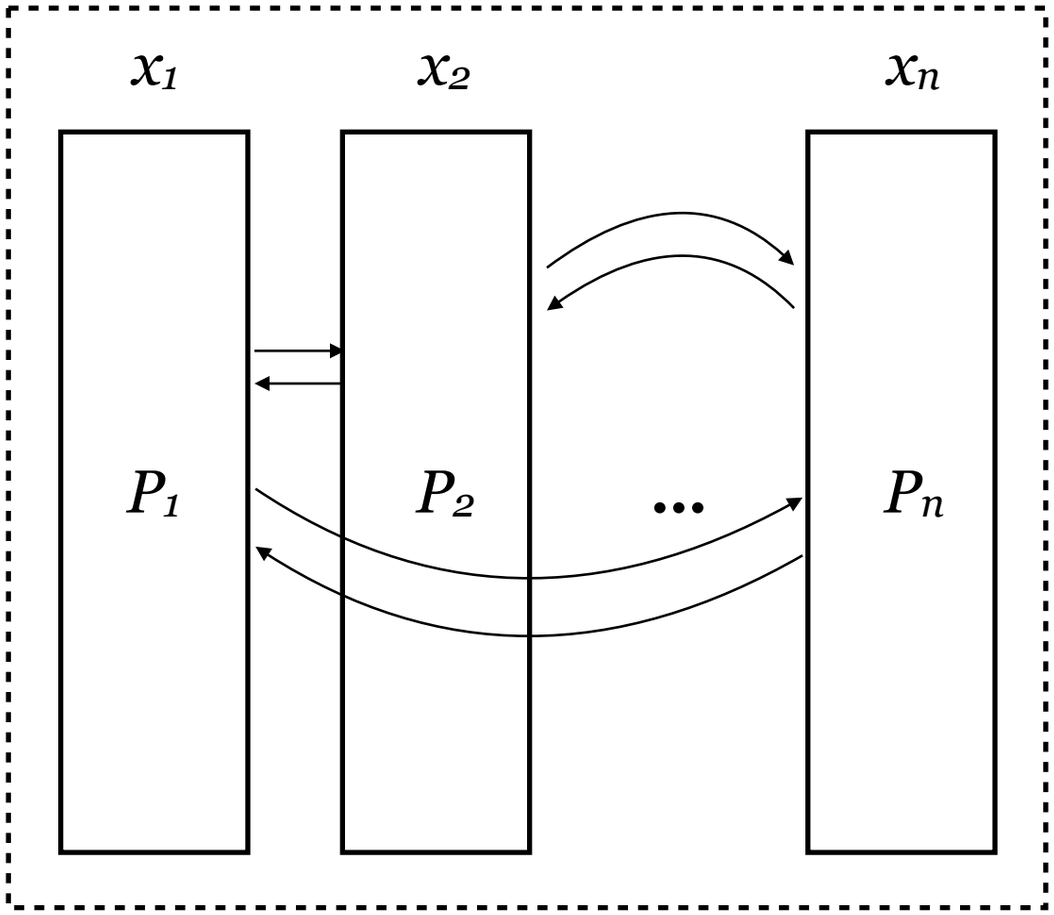
- *(p,e)*-random probing attacks

Starting Point:
t-out-n Secure MPC

$\Pi(C)$



$\widehat{C}$



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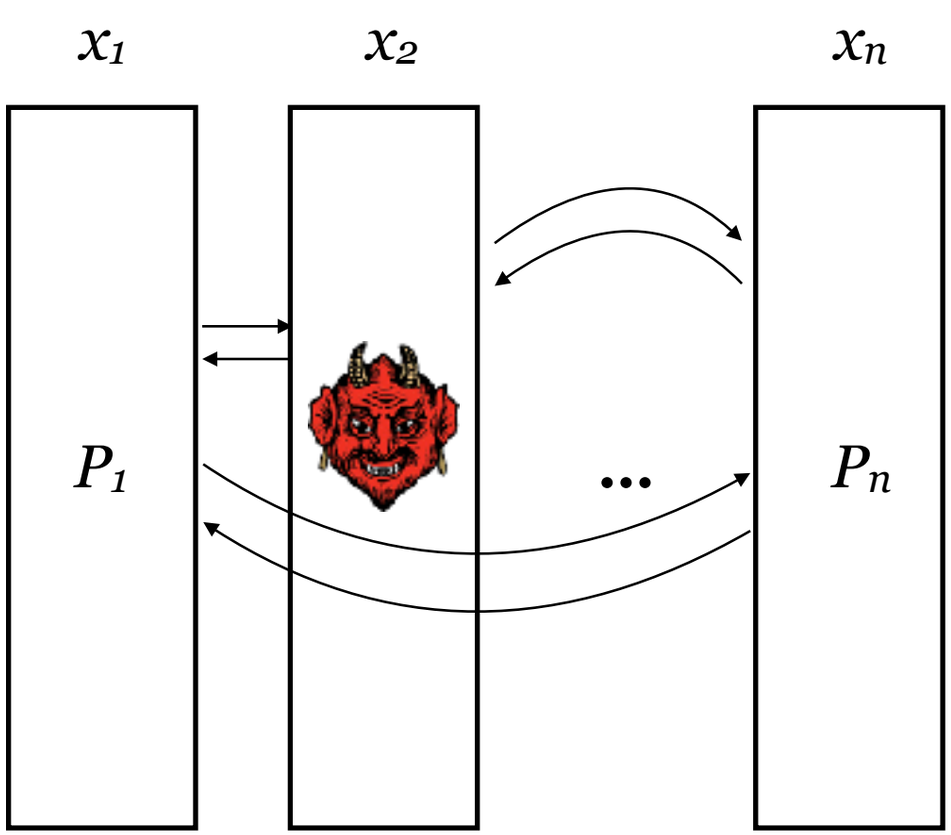
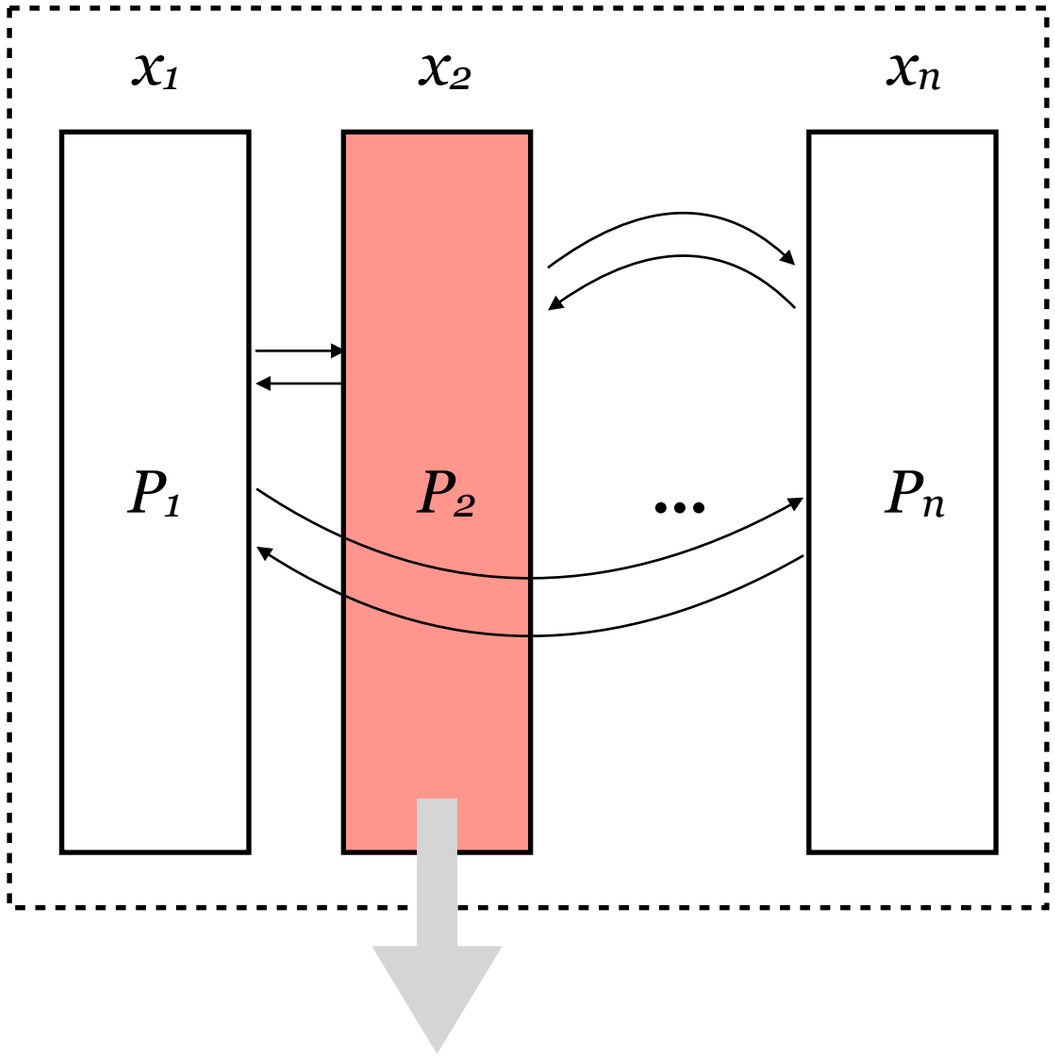


Passive Corruption of P2

$\equiv$

$\widehat{C}$



Leak State of P2

Leakage-Resilient Circuit Compiler

$$\widehat{C} = \Pi(C')$$

C'

Input: shares of x
Output: shares of C(x)

- *reconstruct x*
- *compute C(x)*
- *share C(x)*

Leakage-Resilient Circuit Compiler

Security?

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If at most t wires leaked then the leakage can be simulated

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Probability that more than t wires are leaked = Simulation error e

$$\underset{e}{\text{Simulation Error}} \leq exp\left(\frac{-(1+t)^2}{12\text{poly}(|C|)\cdot p}\right) \qquad \text{(by Chernoff)}$$

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negligible??

If p, $|C|$, t are constants then e is ~~constant~~

(p,e_o)-Base Gadget G_o

Leakage-resilient circuit compiler

with

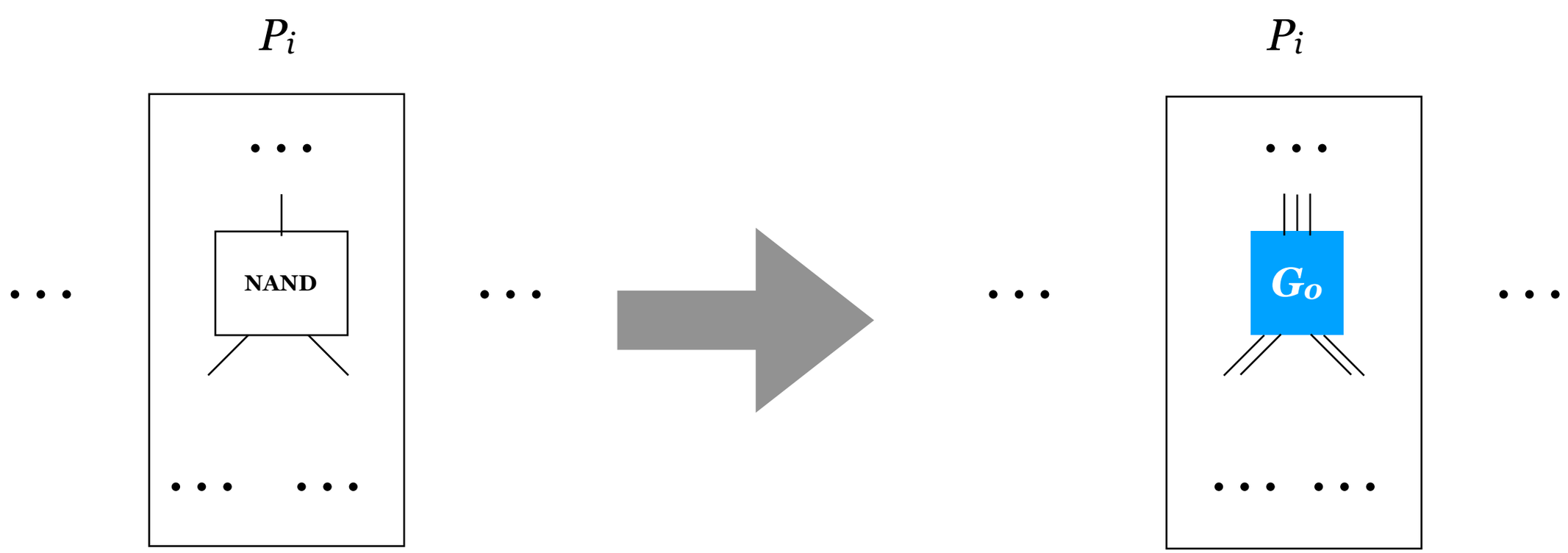
p = constant, $\mathbf{e_o}$ = constant

Reducing the Error

IDEA

- Start with t-out-n secure MPC

- Emulate every gate in t-out-n secure MPC with (p,e_o)-base gadget G_o



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$$\text{Simulation Error } e_1 \leq exp\left(\frac{-(1+t)^2}{12\text{poly}(|C|)\cdot e_0}\right)$$

(by Chernoff)

Size?

Size?

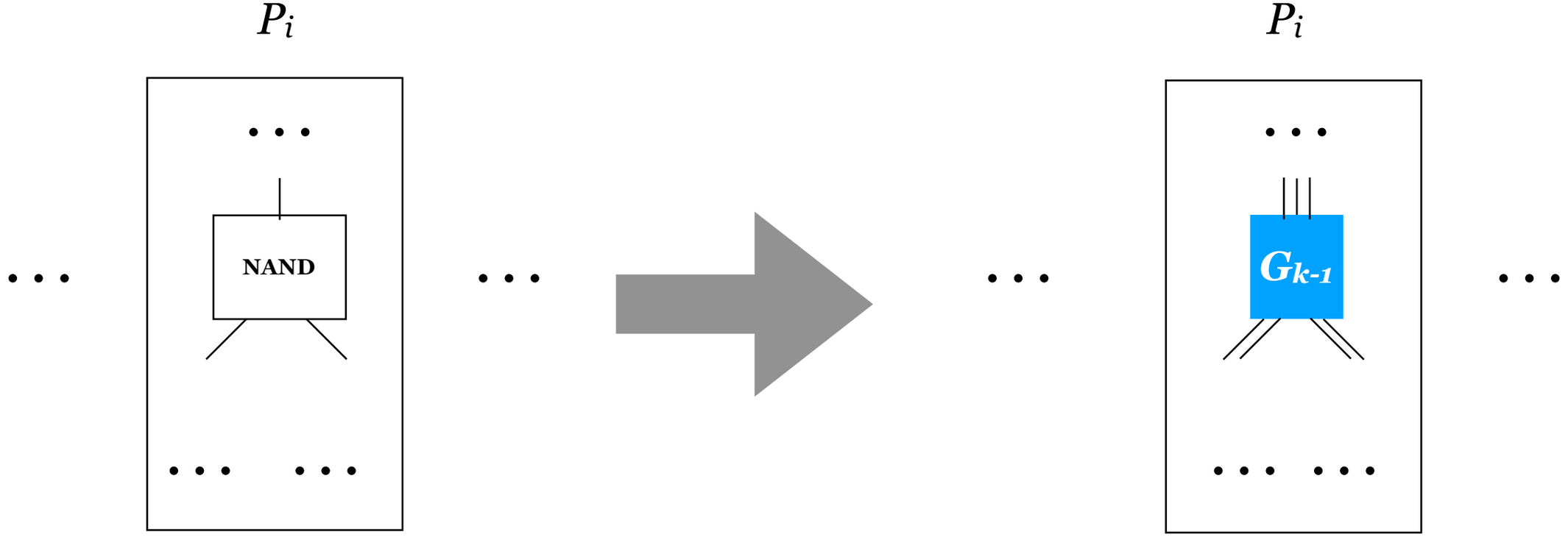
$$|\textbf{Base Gadget}| \times |\Pi(C')|$$

After k steps

IDEA

- Start with t-out-n secure MPC

- Emulate every gate in t-out-n secure MPC with (p,e_{k-1})-gadget G_{k-1}



After k steps: size?

$$\begin{aligned}
\text{Size of } k^{th} \text{ Gadget } G_k &\leq |(k-1)^{th} \textbf{ Gadget}| \times |\Pi(C')| \\
&\leq |(k-2)^{th} \textbf{ Gadget}| \times |\Pi(C')| \times |\Pi(C')| \\
&\cdots \\
&\leq (|\Pi(C')|)^k
\end{aligned}$$

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$$\cdots$$

$$\leq (|\Pi(C')|)^k$$

$$= exp(O(k))$$ *When |C| is a constant...*

After k steps: error

$$\text{Simulation Error } e_k \leq exp\left(\frac{-(1+t)^2}{12\text{poly}(|C|)\cdot e_{k-1}}\right)$$

$$\leq exp\left(\frac{-(1+t)^2}{12\text{poly}(|C|)\cdot exp\left(\frac{-(1+t)^2}{12\text{poly}(|C|)\cdot e_{k-2}}\right)}\right)$$

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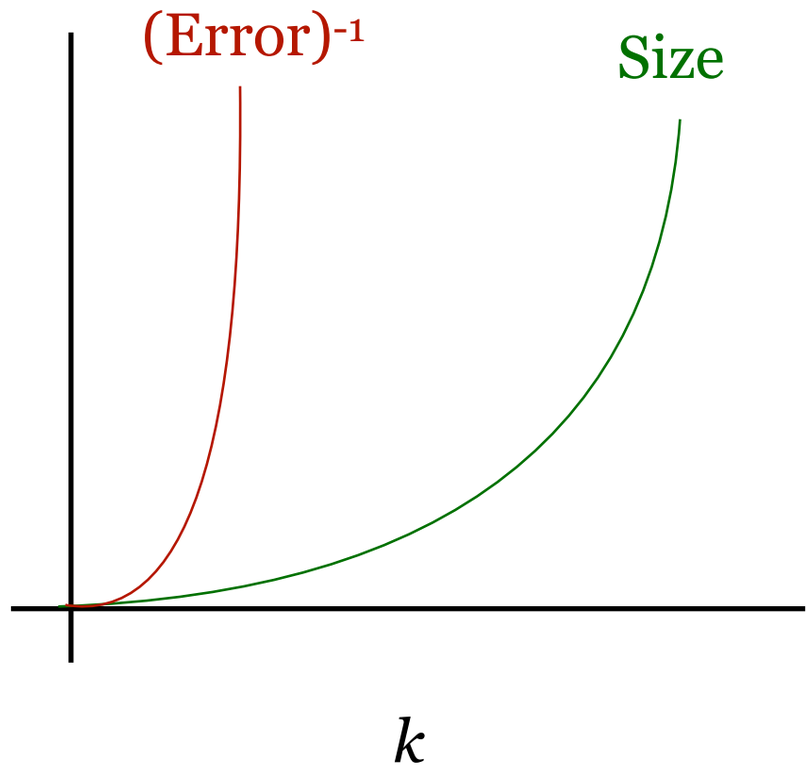
...

$$\leq exp(-2^{O(k)})$$ *When |C| is a constant...*

When |C| is constant,

$$e_k \leq exp(-2^{O(k)})$$

$$\begin{matrix}\text{Size of} \\ k^{th}\text{ Gadget } G_k\end{matrix} \leq exp\left(O(k)\right)$$

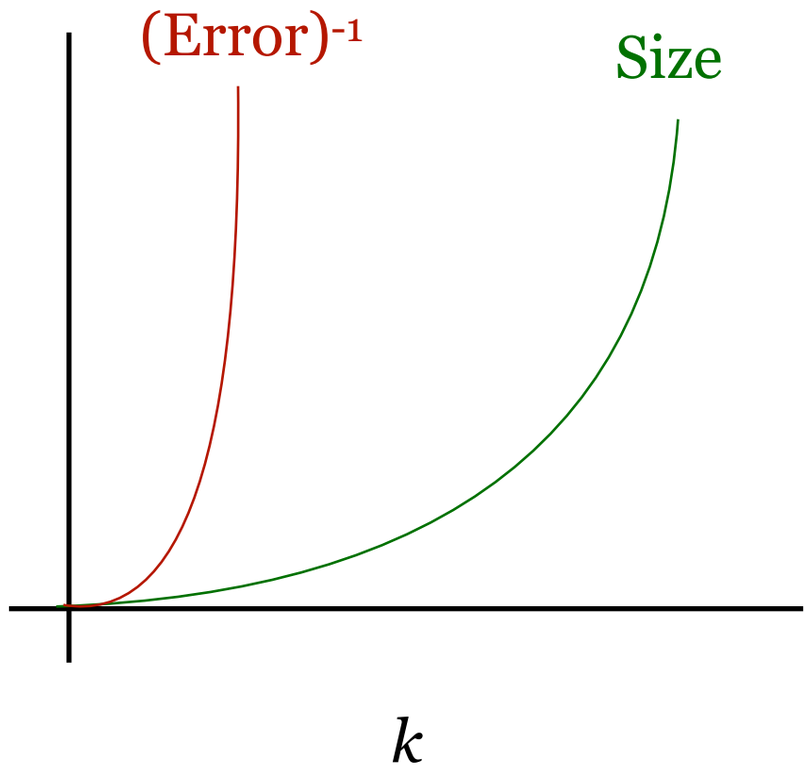


When |C| is constant,

$$\boxed{k = \log(|C|)}$$

$$e_k \leq exp(-2^{O(k)}) = \text{negl}(|C|)$$

$$\text{Size of } k^{th} \text{ Gadget } G_k \leq exp\left(O(k)\right) = \text{poly}(|C|)$$



C = NAND

When |C| is constant,

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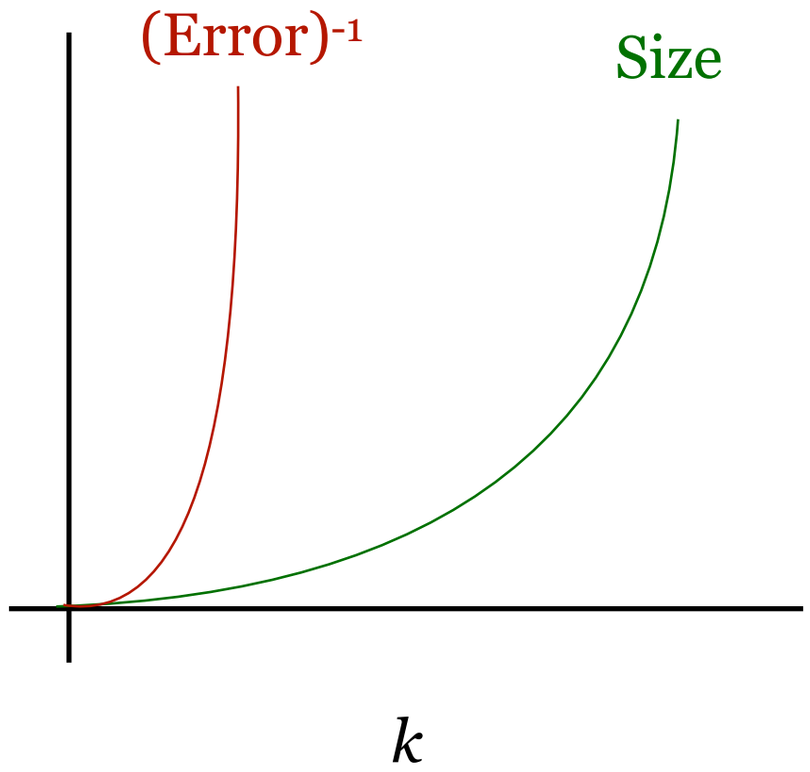
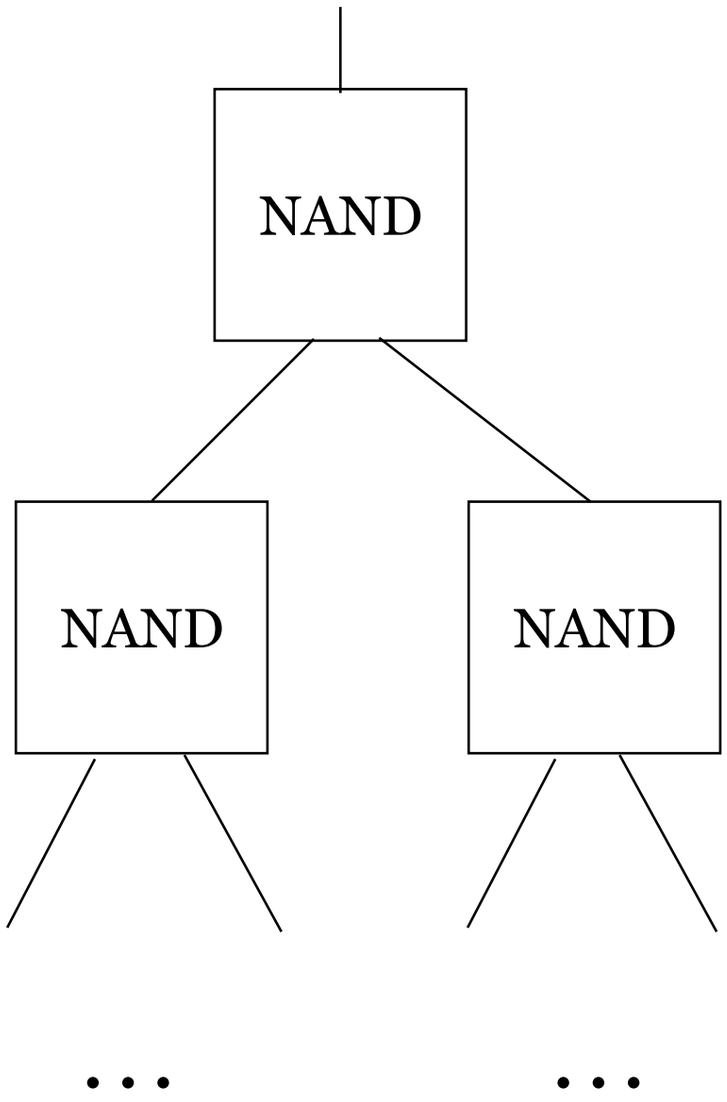


To compile a large circuit C,



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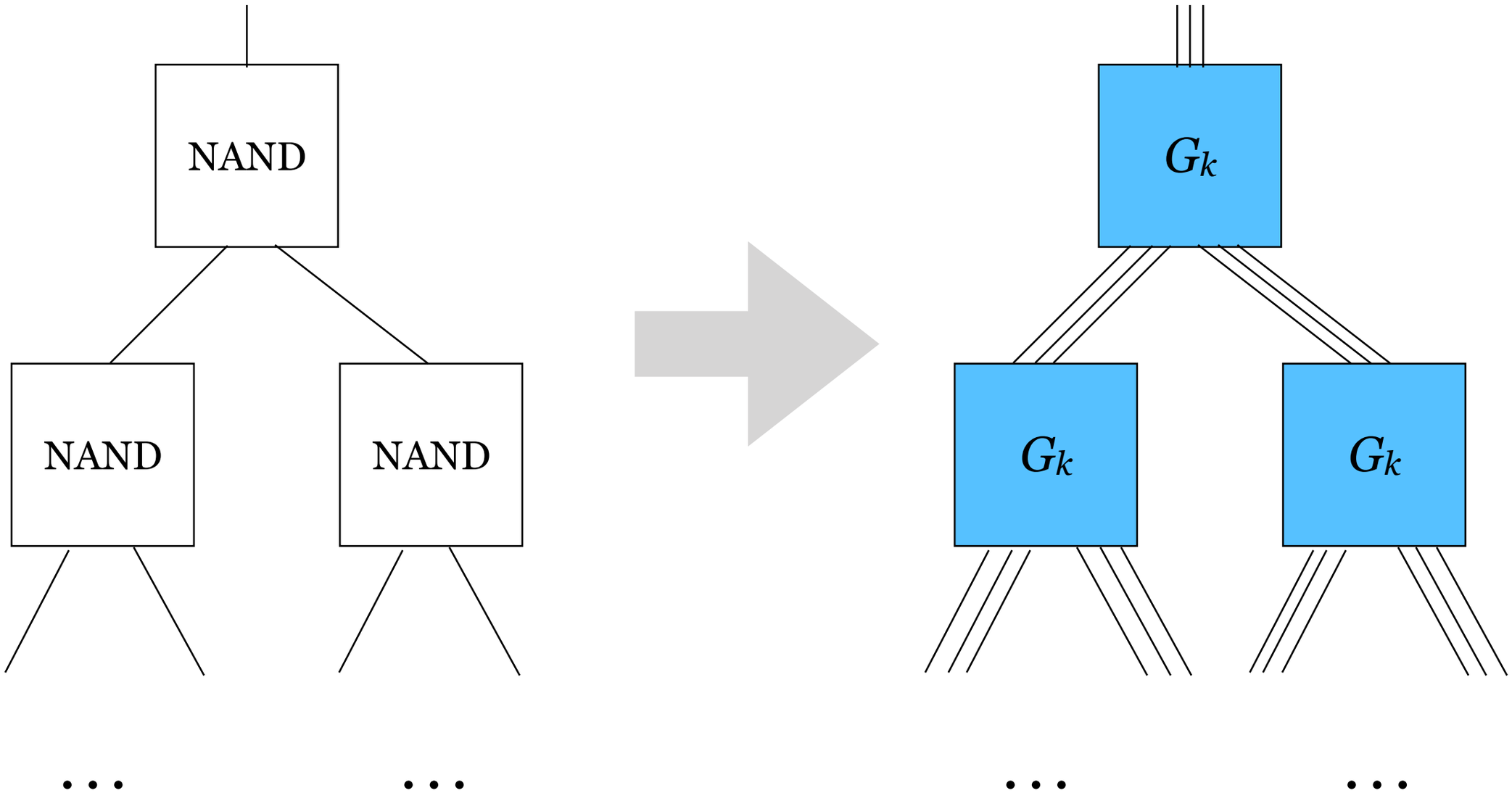
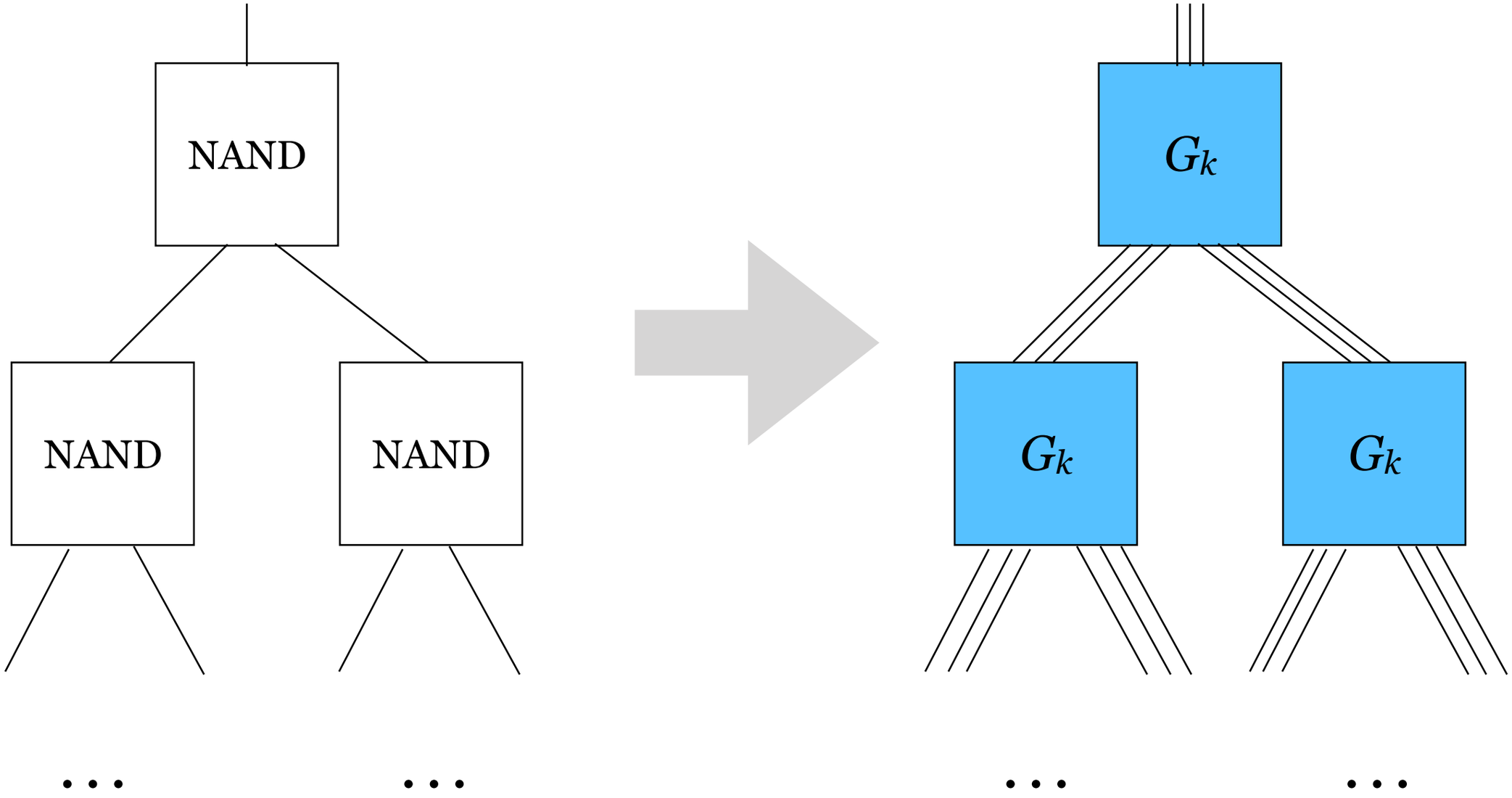


Stitch together the gadgets for every gate in the circuit

To compile a large circuit C,



Compositional issues?

Worst-Case Leakage: t-wire probing

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Worst-Case Leakage: t-wire probing

- Similar approach: analysis much simpler
- Randomness complexity:
  - G_0 has constant randomness locality
  - G_k has randomness locality $O(k)$
  - k=O(log(t))
  - [IKLOPSZ13] “small” randomness locality implies “small” randomness complexity

Conclusion

- Worst-case wire-probing attacks:

  - *Randomness complexity* $t^{1+\varepsilon}$ *(optimal)*

  - *Prior to our work: randomness complexity* $t^{3+\varepsilon}$

- Random wire-probing attacks:

  - *Simpler construction using elementary tools*

Thanks!